REMARKS

Applicant has considered the Office Action dated January 31, 2008, and the references cited therein. Claims 1-13 and 15-17 are currently pending. No claims presently stand allowed. Applicant has amended claims 11 and 17 to address the Section 112 rejections set forth in sections 3-6 of the Office Action, and Applicant has traversed, without amendment, the rejection of claim 12 as being indefinite. All amendments to the original claims are fully supported by the original disclosure of the present application. Applicant has traversed all of the prior art-based rejections of the pending claims for the reasons set forth herein below.

Applicant requests favorable reconsideration of the Office Action's grounds for rejecting the previously pending claims in view of Applicant's amendments to the previously pending claims and the Remarks provided herein below.

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Summary of the Rejections

1. Claim 17 is rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

2. Claims 11, 12 and 17 are rejected under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject-matter which applicant regards as the invention.

3. Claims 1-3, 5-7, 9, 13 and 15-17 are rejected under 35 U.S.C. §103(a) as obvious over Cohen et al. U.S. Patent No. 5,115,506 (Cohen).

4. Claim 4 is rejected under 35 U.S.C. §103(a) as being obvious over Cohen in view of Petolino, Jr., et al. U.S. Patent No. 5,958,041 (Petolino).

5. Claim 8 is rejected under 35 U.S.C. §103(a) as being obvious over Cohen in view of Patterson et al. (Computer Organization & Design: The Hardware/Software Interface)(Patterson).

6. Claim 10 is rejected under 35 U.S.C. §103(a) as being obvious over Cohen in view of Nguyen et al. U.S. Patent No. 5,448,705 (Nguyen).

7. Claim 11 is rejected under 35 U.S.C. §103(a) as being obvious over Cohen in view of Lang et al. (Individual Flip-Flops with Gated Clocks for Low Power Datapaths)(Lang).

8. Claim 12 is rejected under 35 U.S.C. §103(a) as being obvious over Cohen in view of Kleiman U.S. Patent No. 5,515,538 (Kleiman).

Applicant traverses the grounds for each and every rejection for at least the reasons set forth herein below. Applicant addresses the specific rejections in the order they arise in the Office Action.

1. *Rejection of Claim 17 under §112, first paragraph, as failing to comply with the written description requirement*

Applicant traverses the rejection of claim 17 as failing to comply with the written description requirement. Applicant deleted "or the data memory facility" from claim 17. The amendment to claim 17 renders the claim fully supported by the original application. Applicant again refers to the disclosure at paragraph 19 of Applicant's US Pub. No. 2005/0262389.

2. Rejection of Claims 11, 12 and 17 under 35 U.S.C. §112, second paragraph, as being indefinite

Applicant has amended claims 11 and 17 to recite "a" stack pointer and thereby remedy the absence of proper antecedent basis for "stack pointer" in those claims.

Applicant traverses the rejection of claim 12 as indefinite. The Office Action asserts that "the traditional definition of a VLIW instruction is that each slot in the instruction is associated with a specific functional unit in the processor." Applicant respectfully submits that the traditional definition of a VLIW processor does not require that each slot in the instruction is associated with a specific functional unit. The term Very Large Instruction Width (VLIW) indicates that such a processor comprises a plurality of slots for executing distinct portions of an instruction at the same time. Thus a person skilled in the art at the time of the original application filing could construct a VLIW processor from a parallel arrangement of full fledged CPU's -- though cost considerations could possibly lead the skilled person to simplify the architecture of these CPU's (in view of the relative expense of constructing a VLIW processor from full function CPU's).

3. Rejection of Claims 1-3, 5-7, 9, 13 and 15-17 as Obvious Over Cohen

Applicant traverses the obviousness rejection of independent **claim 1** and claims 2, 3, 5-7, 9, 13 and 15-17, which depend from claim 1. The prior art, upon which the obviousness rejection of claim 1 solely relies, neither discloses nor suggests at least one recited element in claim 1. Thus, a *prima facie* case of obviousness has not been established.

The invention recited in claim 1 is directed to a data processor that embodies a new way of handling multiple and nested interrupts using a secondary data storage level. The data processor includes a snapshot buffer for saving a snapshot of processor state information, *including state information from an internal processor pipeline*, during the handling of an interrupt condition, and controller means which saves the contents of the snapshot buffer in a data memory facility having a multi-bit access port facility upon occurrence of a "nested" interrupt condition. Applicant directs specific attention to the portion of amended claim 1 that recites the state information includes *state information from the internal processor pipeline* – supported, for example at paragraph [0003] of Applicant's published application. Thus, in accordance with the invention recited in claim 1, a snapshot is made of the internal processor pipeline state at the time of each interrupt (whether first level or nested). After completing an interrupt, the data processor restores the previous pipeline state from the snapshot buffer. In the case of a nested interrupt, the claimed control means transfers the contents of the snapshot buffer to the data memory (including a multibit access port). Cohen neither discloses nor suggests the above-recited elements of the claimed data processor.

The Cohen reference discloses a microprocessor including three classes of registers: those which are always duplicated and stacked automatically (the unprimed and prime registers); those which are duplicated, but only stacked as necessary and under software control; and those which are not duplicated and are stacked only if necessary and under software control (the other registers.) *See, e.g.*, Cohen, col. 5, lines 8-15. Thus, only the content of the prime and unprimed registers is duplicated and saved on a stack automatically. The unprimed and prime registers comprise a status register SR, a context switch control register, and a program counter PC. *See*, Cohen, col. 3, lines 29-45. Cohen does not disclose or suggest storing the results of the *internal processor pipeline*, as presently recited in the claims.

Cohen does not disclose or suggest Applicant's claimed snapshot buffer which, during the handling of an interrupt condition, accommodates saving state information of various processor state elements "including state information from the internal processor pipeline." In fact, the only state information that Cohen discloses is state information that is the result of operations carried out by the processor. Cohen teaches that the prime 22 and unprime 20 registers are the only registers whose contents are automatically placed on a stack during multiple overlapping (i.e., nested) interrupt conditions. (Cohen, col. 4, lines 25-48). The prime and unprimed registers comprise a status register SR, a context switch control register CSC and a program counter PC (col. 3, lines 29-45). Cohen does not disclose the details of the content of the status register SR, but does make reference to the Motorola 68000 series of microprocessors. As can be seen on page 364 of the product specification for a 68000 processor, attached hereto as Exhibit A, the upper byte of the status register is available to the programmer and, therefore, the result of operations carried out by the processor and not from the internal processor pipeline. Therefore, Applicant respectfully submits that claim 1 is not anticipated by Cohen for at least this reason.

The Office Action concedes that Cohen does not explicitly disclose a system including a processor pipeline. The Office Action asserts it "would have been obvious to one having ordinary skill in the art to save state information from an internal pipeline in response to an interrupt condition. Applicant respectfully traverses this assertion. Interrupts are generally handled by software rather than hardware. The software interrupt handling approach limits programmers to saving context data from registers visible to a programmer. There is no teaching or suggestion in Cohen regarding the storing of the non-visible data contents of internal pipeline registers. For at least this reason, the claimed invention is not obvious over Cohen.

Furthermore, Cohen's architecture differs substantially from Applicant's claimed interrupt handling architecture. According to Cohen (col. 3, lines 13-15) the CPU has a normal and an alternate register set, and the CPU accesses either the normal or the alternate register set. Contrary to Cohen's normal and alternate register sets, Applicant's claimed processor has a snapshot buffer that saves all state information. The snapshot buffer is not accessed by the CPU, and this claimed architecture enables an interrupt within a single clock cycle. In order to enable a single clock cycle interrupt in the processor of Cohen, the

processor would need a dual data path in the processor pipeline, one for its state information during normal processing and the other for its state information during interrupt processing. No indication or suggestion is given in Cohen of the existence of such dual data path.

Claims **2, 3, 5-7, 9, 13 and 15-17** are dependent from claim 1, and therefore Applicant respectfully submits that these claims are not rendered obvious by Cohen for at least the reason that each of the dependent claims (from independent claim 1) includes at least one element that is not disclosed or suggested in Cohen in view of the state of the art.

4-8. Rejection of Claims 4, 8, and 10-12 as being obvious over Cohen in view of various prior art references (i.e., Petolino, Patterson, Nguyen, Lang, and Kleiman

Claim 1 is not rendered obvious by Cohen at least because Cohen does not disclose or suggest the above-identified/discussed missing claim elements. The identified missing claim elements are also not disclosed or suggested by the various secondary references cited in the Office Action in support of the rejections of **claims 4, 8, and 10-12**. Therefore, Applicant respectfully submits that claims 4, 8, and 10-12, are not rendered obvious by the identified combinations of prior art references.

Applicant furthermore notes, with respect to the rejection of **claim 12**, the Office Action asserts a person having ordinary skill in the art will recognize that the interrupt handling techniques of Cohen are applicable to a VLIW processor and will have the same benefits. Applicant respectfully submits that Cohen's teachings give the skilled artisan no incentive to apply its teaching to a VLIW processor. Even if one skilled in the art decided to apply Cohen's disclosed interrupt handling technique to a VLIW type processor, the skilled artisan would not have any teaching regarding how to do this. In the absence of such directions one skilled in the art would simply apply the interrupt technique to any one of the functional units.

The Office Action also asserts that "Kleiman discloses a system in which dedicated hardware is used for interrupt handling." Such hardware can not be found in Kleiman. As described with reference to Figure 2, at col. 7, lines 61-64 kernel threads are scheduled and dispatched on any of the CPU's. Accordingly, Kleiman explicitly teaches away from the present invention, in that the CPU's are not dedicated to a particular task, let alone that there is a CPU dedicated to interrupt processing. No other hardware dedicated to interrupt

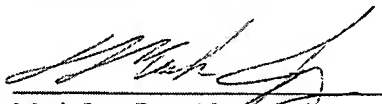
processing can be identified in the processor of Kleiman. It is remarked in the Office Action that only special kernel threads are used to perform interrupt handling, therewith indicating the text portions col. 7, line 60 – col. 8, line 17, col. 9, lines 10-23 and col. 10 lines 16-17. As mentioned in Kleiman, col. 3, lines 5-6, a thread, however, is not a piece of hardware. A thread is merely a sequence of instructions.

In view of the above additional reasons, Applicant respectfully submits that claim 12 is not obvious over Cohen in view of Kleiman.

Conclusion

Applicant respectfully submits that the patent application is in condition for allowance. If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,



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